What is claimed is:

1. A method comprising:

setting a first flag in a first clock domain to indicate availability of data;

setting a second flag in a second clock domain to indicate stability of the data; and

transferring the data between debug controller circuitry clocked in the first domain and processor circuitry clocked in the second domain in response to the setting of the second flag.

2. The method of claim 1, further comprising clearing the first and second flags to indicate completion of the transfer of the data.

3. The method of claim 2, wherein the first flag is stored in a first flip-flop clocked in the first clock domain, and the second flag is stored in a second flip-flop clocked in the second clock domain, the method further comprising clearing the first flag in response to clearing of the second flag.

4. The method of claim 1, wherein transferring the data includes transferring scan chain data.

5. The method of claim 4, wherein transferring the data includes transferring the data between a debug controller circuitry in the form of a JTAG-compatible test access port (TAP) and the processor circuitry.

6. The method of claim 1, further comprising setting an overflow flag in the event the first flag is not cleared prior to an attempted transfer of additional data between the debug controller circuitry clocked in the first domain and the processor circuitry clocked in the second domain.

7. The method of claim 1, further comprising transferring the data in real time between the debug controller circuitry and the processor circuitry without halting operation of the processor circuitry.

8. The method of claim 1, wherein the debug controller circuitry includes a JTAG-compatible test access port (TAP), the method further comprising transferring the data between the debug controller circuitry and the processor

circuitry with a single pass through the JTAG Capture, Shift, and Update data register states.

9. The method of claim 1, further comprising delaying the setting of at least one of the first and second flags for a number of clock cycles sufficient to ensure that the data has reached a stable state.

10. An apparatus comprising:

a first register that sets a first flag in a first clock domain to indicate availability of data;

a second register that sets a second flag in a second clock domain in response to the setting of the first flag to indicate stability of the data; and

a third register that transfers the data between debug controller circuitry clocked in the first domain and processor circuitry clocked in the second domain in response to the setting of the second flag.

11. The apparatus of claim 10, further comprising logic circuitry that clears the first and second flags to indicate completion of the transfer of the data.

12. The apparatus of claim 11, wherein the first flag is stored in a first flip-flop clocked in the first clock domain, and the second flag is stored in a second flip-flop clocked in the second clock domain, the system further comprising circuitry that clears the first flag in response to clearing of the second flag.

13. The apparatus of claim 10, wherein the data includes scan chain data.

14. The apparatus of claim 13, wherein the debug controller circuitry includes a JTAG-compatible test access port (TAP).

15. The apparatus of claim 10, further comprising logic circuitry that sets an overflow flag in the event the first flag is not cleared prior to an attempted transfer of additional data between the debug controller circuitry clocked in the first domain and the processor circuitry clocked in the second domain.

16. The apparatus of claim 10, wherein the third register is adapted to transfer the data in real time between the

debug controller circuitry and the processor circuitry without halting operation of the processor circuitry.

17. The apparatus of claim 10, wherein the debug controller circuitry includes a JTAG-compatible test access port (TAP), and the first, second, and third registers are arranged to transfer the data between the debug controller circuitry and the processor circuitry with a single pass through the JTAG Capture, Shift, and Update data register states.

18. The apparatus of claim 10, further comprising delay circuitry that delays the setting of at least one of the first and second flags for a number of clock cycles sufficient to ensure that the data has reached a stable state.

19. A system comprising:

a flash memory device;

a processor coupled to the flash memory device;

a first register that sets a first flag in a first clock domain to indicate availability of data;

a second register that sets a second flag in a second clock domain in response to the setting of the first flag to indicate stability of the data; and

a third register that transfers the data between debug controller circuitry in the first domain and the processor in the second domain in response to the setting of the second flag.

20. The system of claim 19, further comprising logic circuitry that clears the first and second flags to indicate completion of the transfer of the data.

21. The system of claim 20, wherein the first flag is stored in a first flip-flop clocked in the first clock domain, and the second flag is stored in a second flip-flop clocked in the second clock domain, the system further comprising circuitry that clears the first flag in response to clearing of the second flag.

22. The system of claim 19, further comprising logic circuitry that sets an overflow flag in the event the first flag is not cleared prior to an attempted transfer of additional data between the debug controller circuitry

clocked in the first domain and the processor circuitry clocked in the second domain.

23. The system of claim 19, wherein the third register is adapted to transfer the data in real time between the debug controller circuitry and the processor circuitry without halting operation of the processor circuitry.

24. The system of claim 19, wherein the debug controller circuitry includes a JTAG-compatible test access port (TAP), and the first, second, and third registers are arranged to transfer the data between the debug controller circuitry and the processor circuitry with a single pass through the JTAG Capture, Shift, and Update data register states.

25. The system of claim 19, further comprising delay circuitry that delays the setting of at least one of the first and second flags for a number of clock cycles sufficient to ensure that the data has reached a stable state.